Application Note AN2027

Using the PSoC Microcontroller External Crystal Oscillator

By: Jeff Dahlin
Associated Project: No
Associated Part Family: CY8C25xxx, CY8C26xxx

Summary
The External Crystal Oscillator in the PSoC™ device has specific requirements for correct operation in different configurations. This Application Note details these requirements.

Introduction
The PSoC device's External Crystal Oscillator (ECO) can be used directly as the reference for time keeping or other low speed (<32 kHz) operations. It can also act as the reference for the phase-lock looped mode of the Internal Main Oscillator (IMO) for operations that require an accurate higher speed clock, such as DTMF generation and serial communications. Optimal performance from the ECO for each of these functions requires different external components and different control register settings.

Global Resources	
CPU_Clock	24_MHz
32K_Select	External
PLL_Mode	Disable
Sleep_Timer	512_Hz
24V1= 24MHz/N	4
24V2= 24V1/N	1
Analog Power	SC On/Ref Low
Ref Mux	(Vcc/2)+/-BandGap
Op-Amp Bias	Low
A_Buff_Power	Low
SwitchModePump	OFF
VoltMonRange	5.0V
VoltMonThreshold	80%
Supply Voltage	5.0V

Figure 1: 32K_Select Setting for ECO Operation

External Crystal Oscillator Basics
The source for the PSoC 32K clock can be the low accuracy Internal Low-speed Oscillator (ILO) or the higher accuracy External Crystal Oscillator (ECO). The 32K Select bit of the Oscillator Control 0 Register (OSC_CR0) determines which source is used. The simplest way to set this bit is to set the "32K_Select" parameter in the Global Resources grid of PSoC Designer to "External" (highlighted in Figure 1).

The ECO drive circuitry must be connected to a 32,768 Hz watch crystal through the XTALIn and XTALOut pins of the PSoC MCU.

The XTALIn and XTALOut pins must have their drive modes set to High Z (highlighted in Figure 2) for the ECO to work properly. If the pins' drive modes are not set to High Z, the drive circuitry will free-run at an incorrect frequency.

Port	Select	Drive
P0[3]	StdCPU	Pull Down
P0[4]	StdCPU	Pull Down
P0[5]	StdCPU	Pull Down
P0[6]	StdCPU	Pull Down
P0[7]	StdCPU	Pull Down
P1[0]	StdCPU	High Z
P1[1]	StdCPU	High Z
P1[2]	StdCPU	Pull Down
P1[3]	StdCPU	Pull Down
P1[4]	StdCPU	Pull Down

Figure 2: XTALIn and XTALOut Pin Drive Settings for ECO Operation

ECO Operation

The ECO operates as a low power oscillator. To accomplish this it is designed as a low-amplitude, high-impedance analog circuit. It should be treated as such when placing the components and designing the circuit. Layout is important to performance. Also note that the presence of contaminants on the PCB can impact the performance of the oscillator.

The crystal and the feedback capacitors should be placed as close as is practical to the pins of the microcontroller and should be placed over a common-ground plane. High-speed digital signals (signals with fast fall and rise times) should not be routed close to the ECO circuit. Also, digital signals should not be routed through the ECO external components. When possible, the pins immediately adjacent to the ECO pins should be left unconnected, or they should have lower speed signals connected to them.

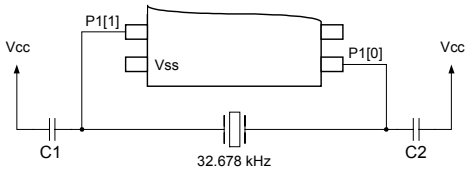

Figure 3: ECO Crystal Connections

Notice that in Figure 3, the feedback capacitors are shown connected to V_{cc}. This is the optimal configuration because the ECO driver is referenced to V_{cc}. If the capacitors are incorrectly connected to V_{ss}, the ECO will operate at the correct frequency, but will be slightly more susceptible to power supply noise.

For standard ECO operation (when not being used as a reference for the Internal Main Oscillator PLL), the configurations described in the CY8C25xxx/26xxx Family Data Sheet should be used.

- 32.768 kHz, 12.5 pF, 1µW watch crystal
- NPO ceramic capacitors
- C1 = C2 = 25 pF – C_P – C_B

Where C1 and C2 are the ECO feedback crystals shown in Figure 3, C_P is the package capacitance and C_B is the board capacitance.

The package capacitances for the various PSoC device packages can be found in the Clocking section of the CY8C25xxx/26xxx Data Sheet.

The board capacitance will depend on PCB geometry, but for example, a layout with 0.20" long, 0.010" wide traces over a ground plane on a 4-layer 0.062" thick PCB, has a board parasitic capacitance of 0.3 pF on each pin.

Table 1 shows standard capacitor values that can be used for C1 and C2 with the various PSoC microcontroller packages, assuming the 0.3 pF board capacitance in the previous example.

Table 1: ECO Capacitor Values for Balanced Feedback

Package	Typical C_P	C1	C2
8 PDIP	0.9 pF	22 pF	22 pF
20 PDIP	2.0 pF	22 pF	22 pF
20 SOIC	1.0 pF	22 pF	22 pF
20 SSOP	0.5 pF	22 pF	22 pF
28 PDIP	2.0 pF	22 pF	22 pF
28 SOIC	1.0 pF	22 pF	22 pF
28 SSOP	0.5 pF	22 pF	22 pF
44 TQFP	0.5 pF	22 pF	22 pF
48 PDIP	5.0 pF	20 pF	20 pF
48 SSOP	0.6 pF	22 pF	22 pF

ECO and PLL Lock Mode

The Internal Main Oscillator (IMO) can be configured to Phase Lock Loop (PLL) to the ECO. This will result in an IMO with more accurate frequency and less voltage and temperature drift than can be accomplished with the Internal Main Oscillator alone.

When using the PLL configuration of the IMO, an unbalanced feedback capacitor configuration and a local bypass capacitor, as described in the following sections, must be used for proper operation.

The PLL Mode bit of the OSC_CR0 register enables the PLL lock mode of the IMO. The simplest way to set this bit is to set the "PLL_Mode" parameter to "Ext Lock" in the Global Resources window of PSoC Designer (highlighted in Figure 4).

In general, a PLL requires a low-jitter reference in order to remain stable, and because the PSoC microcontroller's ECO uses a low-amplitude signal, the presence of noise will cause the position of the clock edges to jitter from cycle to cycle. The base frequency of the ECO will remain accurate but the jitter can cause the IMO to be unstable.

When using the PLL mode of the Internal Main Oscillator (IMO), PCB layout is the most critical factor in minimizing jitter on the ECO. By carefully designing the PCB, the amount of noise present in the ECO circuit can be minimized. But there are other required changes that increase the stability of the ECO. These include using unbalanced feedback capacitors, providing a local V_{cc} bypass, and increasing the ECO drive current.

Global Resources	
CPU_Clock	24_MHz
32K_Select	External
PLL_Mode	Ext Lock
Sleep_Timer	512_Hz
24V1= 24MHz/N	4
24V2= 24V1/N	1
Analog Power	SC On/Ref Low
Ref Mux	(Vcc/2)+/-BandGap
Op-Amp Bias	Low
A_Buff_Power	Low
SwitchModePump	OFF
VoltMonRange	5.0V
VoltMonThreshold	80%
Supply Voltage	5.0V

Figure 4: PLL_Mode Setting for IMO Operation

Use of Unbalanced Feedback Capacitors

By using an unbalanced pair of feedback capacitors, the amplitude of the input signal can be increased. This will reduce the ECO's noise susceptibility. In this case, the series capacitance of the feedback capacitors still needs to be 12.5 pF. An unbalanced pair of capacitors will cause an increase in the operating current and will not improve the performance of the ECO, so this change is not recommended for standard ECO operation.

The capacitance on each pin is comprised of the package capacitance, in parallel with the board parasitic capacitance, in parallel with the external capacitor (see Equations 1 and 2).

$$C_{P1.1} = C1 + C_B + C_P$$

Equation 1: XTALIn (Port 1, Pin 1) Capacitance

$$C_{P1.0} = C2 + C_B + C_P$$

Equation 2: XTALOut (Port 1, Pin 0) Capacitance

For this configuration, the total capacitance on the XTALOut (Port 1, Pin 0) should be near 100 pF. Equation 3 shows the total capacitance at the XTALOut pin ($C_{P1.0}$) if a 100 pF capacitor is used.

$$C_{P1.0} = 100\,pF + C_P + C_{B0}$$

Equation 3: XTALOut (Port 1, Pin 0) Capacitance

(Where C_P is the package capacitance and C_{B0} is the board parasitic capacitance on XTALOut.)

The feedback capacitor at the XTALIn pin should be calculated so that the series capacitance at the crystal pins totals 12.5 pF. Equation 4 shows the calculation for the ideal value of C1 (the capacitor on P1[1] XTALIn).

$$C1 = \frac{(C2 + C_P + C_{B0}) \cdot 12.5\,pF}{(C2 + C_P + C_{B0}) - 12.5\,pF} - C_P - C_{B1}$$

Equation 4: XTALIn (Port 1, Pin 1) Capacitance

(Where C_P is the package capacitance and C_{B1} is the board parasitic capacitance on XTALIn.)

Table 2 lists typical package capacitances, and standard capacitor values for C1 and C2 closest to the calculated ideal values for various packages. Board parasitic capacitance values of 0.3 pF were used in these calculations.

Table 2: ECO Capacitor Values for Unbalanced Feedback

Package	Typical C_P	C1	C2
8 PDIP	0.9 pF	12 pF	100 pF
20 PDIP	2.0 pF	12 pF	100 pF
20 SOIC	1.0 pF	12 pF	100 pF
20 SSOP	0.5 pF	12 pF	100 pF
28 PDIP	2.0 pF	12 pF	100 pF
28 SOIC	1.0 pF	12 pF	100 pF
28 SSOP	0.5 pF	12 pF	100 pF
44 TQFP	0.5 pF	12 pF	100 pF
48 PDIP	5.0 pF	9 pF	100 pF
48 SSOP	0.6 pF	12 pF	100 pF

An error of 1 pF in C1 or C2 will result in about 3 ppm of additional error in the output frequency.

Provide a Local Bypass

When using the PLL configuration of the IMO additional filtering of the V_{cc} power is required. For this purpose a local V_{cc} bypass capacitor is add at the XTALIn pin (Port 1, Pin 1). To do this, configure the pin's drive mode to be Strong and write a 1 to the Data Register (PRT1DR). Connect the pin to V_{cc} and connect a 0.1 µF capacitor between the pin and V_{ss}. This will connect the internal power bus to V_{cc} through the pin pull-up FET; providing a local low impedance connection to V_{cc}.

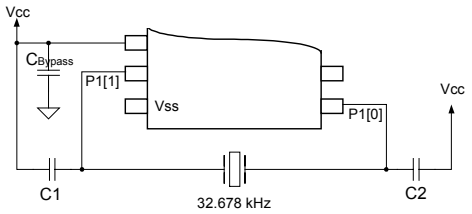

Figure 5: PLL_Mode Connections

Increase the ECO Drive Current

To increase the drive current of the ECO circuit, write a 0x0F to the ECO Trim register (ECO_TR, Bank 1, 0x0F). This is done automatically by *boot.asm* when the "PLL_Mode" parameter is set to "Ext Lock."

Start-up Requirements

Both the ECO and the IMO experience periods of instability when they are first started. Because of this, the output of the ECO should not be used as a source for the internal 32K clock or as a reference for the PLL mode of the IMO until it has had time to stabilize. Additionally, the CPU clock speed must be lowered when the IMO is initially switched to PLL mode to prevent the CPU clock from exceeding its operational limit.

These circumstances require the ECO and the IMO PLL mode to follow a specific start-up sequence. *boot.asm* meets this requirement if the appropriate settings are selected in the Global Resources grid in Device Editor of PSoC Designer.

Starting the ECO

When the ECO is first enabled, its output is not connected to the 32K clock tree within the PSoC microcontroller. Instead, the 32K clock continues to be driven by the Internal Low-speed Oscillator (ILO) until the Sleep Timer reaches terminal count. With this mechanism, the Sleep Timer is used to delay connecting to the ECO until its output has stabilized.

The steps listed below are followed by *boot.asm* when starting the ECO:

1. The Sleep Timer should be set to 1 second and cleared. (The Sleep Timer Interrupt does not have to be enabled.)
2. The ECO should be enabled (set the 32K Select bit of OSC_CR0 to 1).
3. After the Sleep Timer reaches terminal count, the ECO can be used as clock source for event timing.

Starting the IMO PLL Mode

The IMO cannot be phase locked to the ECO until the ECO is stable – approximately one second. Also, there is a maximum CPU clock-frequency restriction (3 MHz) that cannot be exceeded when starting PLL mode. Both of these restrictions are in place to prevent the CPU clock frequency from temporarily exceeding 12 MHz for 3 V operation (or 24 MHz for 5 V operation).

The current version of *boot.asm* (PSoC Designer version 3.20) holds off entry to main( ) until the clocks are stable. This means that calling main will be delayed about one second when using the ECO. The following delays are present in *boot.asm:*

1. Whenever the ECO is enabled, a one-second delay is added in order to wait for the ECO to become stable.
2. Whenever the PLL lock mode of the IMO is enabled, a 16 msec delay is added in order to wait for the IMO frequency to stabilize prior to setting the CPU clock frequency to the designer's setting.

To accurately provide these delays, *boot.asm* uses the Sleep Timer, but does not enable the interrupt. Therefore, *boot.asm* no longer contains a Sleep Timer Interrupt Service Routine (ISR). If a designer needs to add a Sleep Timer ISR, it is recommended that one be created in a separate source code file.

Previous versions of PSoC Designer provided a variable, `ClockNotStable`, which indicated when the clocks were stable. Because main( ) is now not called until the clocks are stable, this variable is no longer provided.

If some tasks must be accomplished before the 1-second period is expired, initialization code could be added to *boot.asm*, or a designer could chose to write their own clock-initialization code as long as the rules in this section are held to.

Notes

1. Setting the "32K_Select" Global Resource to "Internal" and "PLL_Mode" Global Resource to "External Lock" is an invalid configuration. There is no connection from the Internal Low-speed Oscillator to the Internal Main Oscillator (see the Clock Tree diagram in the CY8C25xxx/26xxx Family Data Sheet).

2. The XTALIn and XTALOut pins are also used for the In-System Serial Programming. The pins can be configured to function for both operations in the same design. See Application Note AN2014, *Design for In-System Serial Programming (ISSP™)*, for more information on In-System Programming.

Cypress MicroSystems, Inc.
22027 17th Avenue S.E. Suite 201
Bothell, WA 98021
Phone: 877.751.6100
Fax: 425.939.0999
http://www.cypressmicro.com/ / http://www.cypress.com/aboutus/sales_locations.cfm / support@cypressmicro.com