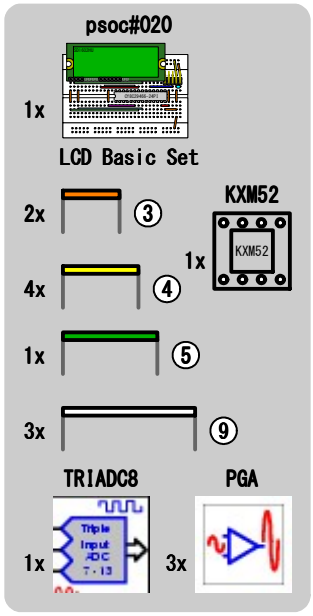
PSoC

15+

022

Gsensor & ADC



Properties - PGA_1

Name	PGA_1
User Module	PGA
Version	3.2
Gain	1.000
Input	AnalogColumn_InputMUX_0
Reference	AGND
AnalogBus	Disable

Gain

Properties - PGA_2

Name	PGA_2
User Module	PGA
Version	3.2
Gain	1.000
Input	AnalogColumn_InputSelect_1
Reference	AGND
AnalogBus	Disable

Gain

Properties - PGA_3

Name	PGA_3
User Module	PGA
Version	3.2
Gain	1.000
Input	AnalogColumn_InputSelect_2
Reference	AGND
AnalogBus	Disable

Gain

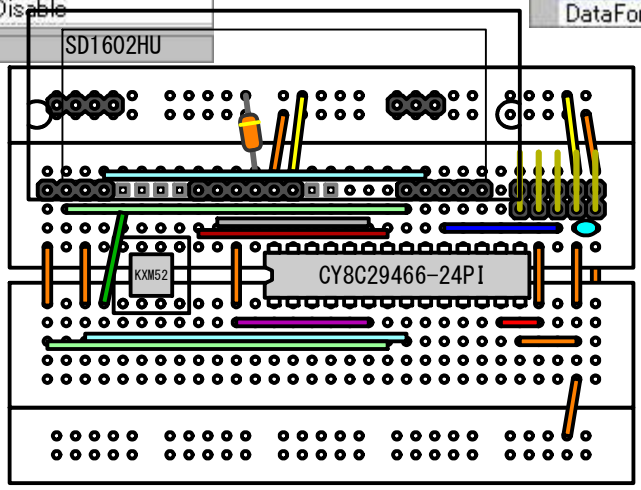
Global Resources - psoc022

Power Setting [V	5.0V / 24MHz
CPU_Clock	SysClk/8
32K_Select	Internal
PLL_Mode	Disable
Sleep_Timer	512_Hz
VC1= SysClk/N	16
VC2= VC1/N	16
VC3 Source	SysClk/1
VC3 Divider	1
SysClk Source	Internal
SysClk*2 Disable	No
Analog Power	SC On/Ref Low
Ref Mux	(Vdd/2)+/-BandGap
AGndBypass	Disable
Op-Amp Bias	Low
A_Buff_Power	Low
SwitchModePump	OFF
Trip Voltage [LVD	4.81V (5.00V)
LVDThrottleBack	Disable
Watchdog Enable	Disable

VC1= SysClk/N

Properties - TRIADC8...

Name	TRIADC8_1
User Module	TRIADC8
Version	1.0
ADC Input1	ACB00
ADC Input2	ACB01
ADC Input3	ACB02
ClockPhase1	Norm
ClockPhase2	Norm
ClockPhase3	Norm
Clock	VC2
DataFormat	Unsigned



090827 by K.I http://bluefish.orz.hm/sdoc/bb_psoc.html

main.c

```
void main()
{
   BYTE gx,gy,gz;

   M8C_EnableGInt ;
   TRIADC8_1_Start(TRIADC8_1_HIGHPOWER);
   TRIADC8_1_GetSamples();

   PGA_1_Start(PGA_1_HIGHPOWER);
   PGA_2_Start(PGA_2_HIGHPOWER);
   PGA_3_Start(PGA_3_HIGHPOWER);
   LCD_1_Start();
   LCD_1_InitBG(LCD_1_SOLID_BG);

   while(1) {
     while(!TRIADC8_1_fIsDataAvailable());
     gz = (gz+TRIADC8_1_cGetData1())/2;
     gx = (gx+TRIADC8_1_cGetData2())/2;
     gy = (gy+TRIADC8_1_cGetData3ClearFlag())/2;

     LCD_1_Position(0,1); LCD_1_PrHexByte(gx);
     LCD_1_DrawBG(1,1,4,gx/12);
     LCD_1_Position(0,6); LCD_1_PrHexByte(gy);
     LCD_1_DrawBG(1,6,4,gy/12);
     LCD_1_Position(0,11); LCD_1_PrHexByte(gz);
     LCD_1_DrawBG(1,11,4,gz/12);
   }
}
```